User Guide for Notebook Debug Card

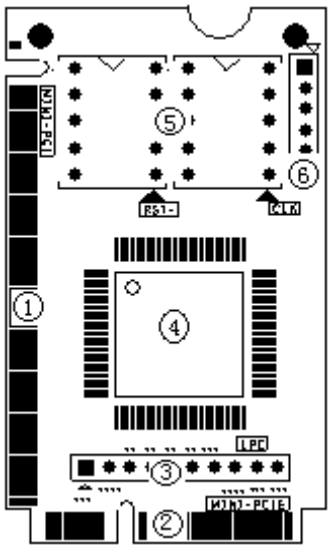
(3 in 1 version)

The model notebook Debug Card supports 3 bus interfaces: **Mini PCI,Mini PCI-E and LPC.** While using it, only connect with one of these 3 interfaces. This product is easy to be used, and is designed with good stability. It is your ideal tool for notebook repair.

Catalogue

➢ 1. **Debug Card structure and components**

(see below chart)



1）Mini PCI interface:

This is used to connect this Debug Card to notebook's Mini PCI slot.

2）Mini PCI-E interface:

This is used to connect this Debug Card to notebook's Mini PCI-E slot.

3）LPC interface:

This is used to connect this Debug Card to notebook's LPC interface.

4）Special Main Chip:

For process Mini PCI,Mini PCI-E,LPC passed signals.

5）Two 7-segment LEDs:

This is used to display the debug code.

6）Test port:

This port is reserved for factory inspection, and end-user should not use this port.

➢ 2.MiniPCI interface

Mini PCI is general use interface of notebook,which function is same as PCI interface.Mini PCI have 124 bus pins in total and this model Debug Card achieves required functions through 101 pins among them.When install this debug card into notebook Mini PCI slot,the length of Debug Card is shorter than the length of notebook Mini PCI Slot.Thus it brings more conveniency to use this debug card on notebooks.

➢ 3.The MiniPCI-E interface in the Debug Card

Mini PCI-E is used as a trend in the notebooks. This Debug Card doesn't use all of the Mini PCI-E

bus pins, and only the below pins are used: PIN-8, PIN-10, PIN-12, PIN-14, PIN-16, PIN-17, and PIN-19. In the Mini PCI-E specifications, those pins are optional, and some notebook manufactures keep those pins unconnected. But more and more notebook manufacturers are using those pins as debug-port, such as IBM, Lenovo,Toshiba, HP, ASUS, TCL and most of "netbook". This Debug Card can only work in the notebooks, which support the Mini PCI-E debug-port. For the notebooks, which don't support the Mini-PCIe debug-port, this debug card Mini PCI-E interface will not work. In this case, you will need to use the LPC port (referring to Part-4: The LPC interface).

➢ 4. The LPC interface in the Debug Card

For the user, whose notebooks don't support the Mini PCI-E debug-port interface, the LPC interface can be used. LPC interface exists in all notebook mainboards. In the Debug Card, from left to right, the LPC definition is:

PIN1-3.3V	PIN2-LFRAME#	PIN3-LAD3	PIN4-LAD2	PIN5-LAD1
PIN6-LAD0	PIN7-GND	PIN8-LRESET#	PIN9-LCLK	PIN10-3.3V

Usually, the notebook boards haven't LPC connectors or slots. And the users will need to connect this LPC port to the notebook by using wires. Below is some description for how to connect the notebook Combo-Debug-Card to your notebook through this LPC interface.

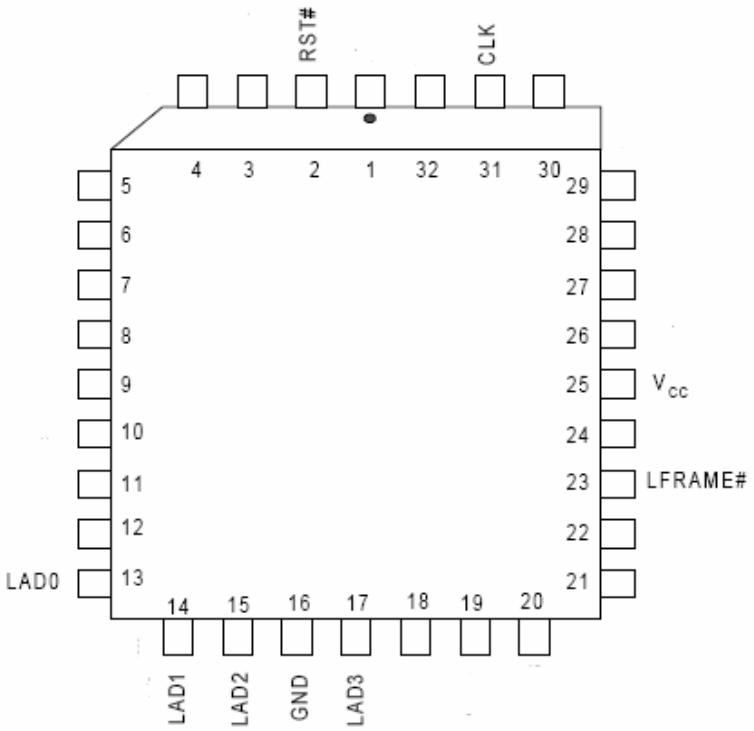
✧ If your notebooks use LPC VBIOS, you can connect the Debug Card to your notebook's BIOS bus.

>> LPC BIOS Pin definition:

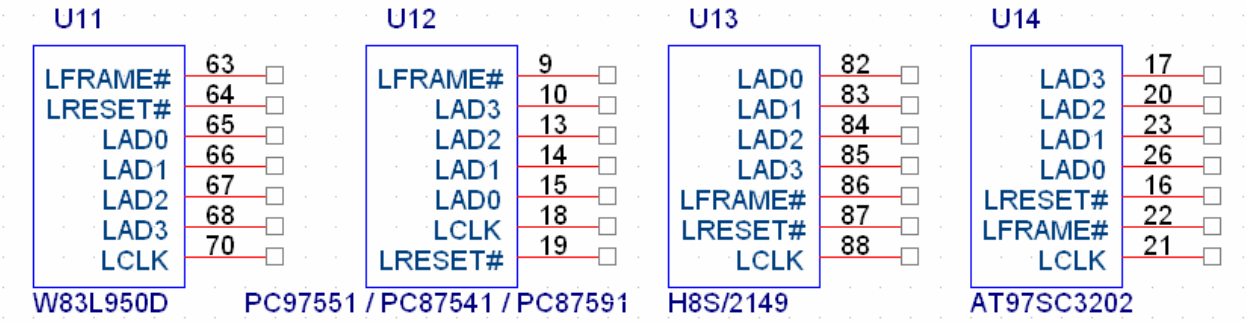
PIN2-RST#	PIN13-LAD0
PIN14-LAD1	PIN15-LAD2
PIN16-GND	PIN17-LAD3
PIN23-LFRAME#	PIN25-VCC
PIN31-CLK	

>>The connection between Debug Card and the notebook's mainboard.

The Debug Card	Notebook BIOS
PIN1-3.3V	PIN25-VCC
PIN2-LFRAME#	PIN23-LFRAME#
PIN3-LAD3	PIN17-LAD3
PIN4-LAD2	PIN15-LAD2
PIN5-LAD1	PIN14-LAD1
PIN6-LAD0	PIN13-LAD0
PIN7-GND	PIN16-GND
PIN8-LRESET#	PIN2-RST#
PIN9-LCLK	PIN31-CLK
PIN10-3.3V	PIN25-VCC



User can connect the Debug Card to any LPC bus. Some LPC interface chips are listed as below:such as PC97551,PC87541,PC87591,H8S/2149,W83L950D,TCPA and etc. You can connect the Debug Card to the corresponding pins. For more information, please refer those chips' datasheets



Note: The above chart don't list out power supply and GND.This Debug Card uses 3.3V as power supply, and you can use any 3.3V and GND signals in your notebook mainboard. Please be aware of that connecting the Debug Card to a non-3.3V power may damage this Debug Card.

✧ For IBM X60 notebooks, the LPC interfaces are located in the U39 slot of the mainboard. The Pin definitions are as below:

A2->LRESET# A3->LFRAME#
A5->LCLK A9->LAD3
A10->LAD2 A11->LAD1
A12->LAD0

✧ For IBM T6, R6 notebooks, the LPC interfaces are located in the J26 slot of the mainboard. The Pin definitions are as below:

A1->LCLK, A3->LFRAME#
B2->LRESET# B7->LAD3

A7->LAD2 B6->LAD1 A6->LAD0

➢ 5. The LED Display in the Debug Card

The Display portion is composed with two 7-segment LEDs.The two dots of two LEDs respectively used to show RST and CLK signals status. When the notebook is in “Reset” status, the left LED dot will be on. And when the notebook Clock work normal,the right LED dot will be on.

When pressing the Reset switch on the notebook, the left LED dot will be on,and the right LED dot is off.

When the notebook is in good work status, the left LED dot will be off,and the right LED dot is on.It shows the notebook ”RST” signal normal,”CLK” signal normal.At the same time,the 7-segment LEDs will show corresponding code.

If the left LED dot is on always,it shows the notebook is in “RST” status.

➢ 6. Part of Error Code explanation

When the notebooks are running, this Debug Card will show the corresponding debug code. If there is a problem in the notebook, you can judge the problem by the debug code. Below is the explanation for some main error codes.

✧ AWARD BIOS:

The explanation when the Debug Card shows the below debug codes.

Code	Explanation	Note
C0	Close cache	
01	Processor test	
07	CMOS test	
C1	Memory size test	
0A	Set the interrupt table	
0C	Initiate the keyboard	
0D	Initiate the Graphic card	
1A	Show CPU frequency	
3C	CMOS setting	
42	Initiate hardware	
52	Test the extended ROM	
FF	Boot	

✧ AMI BIOS:

The explanation when the Debug Card shows the below debug codes.

Code	Explanation	Note
00	Error in self test	
01	Error in processor test	
0D, 0F	Error in CMOS test	
1A 至 22	Error in Memory test	
3A	Error in graphic card	
FF	Pass the self test	

Note:
Please be aware that the debug-codes are dependent on your notebook motherboard BIOS, not the debug card. Even it the same notebook motherboard, if you use different BIOS, the outputted debug codes can be different.

AWARD ELITEBIOS 4.51PG ：EISA 300H； ISA 80H

16		
C0	Turn Off Chipset Cache	Cache
01	Processor Test 1	1
02	Processor Test 2	2
03	Initialize Chips	
04	Test Memory Refresh Toggle	
05	Blank video,Initialize keyboard	
06	Reserved	
07	Test CMOS Interface and Battery Status	CMOS
BE	Chipset Default Initialization	BIOS
C1	Memory Presence test	
C5	Early Shadow	
C6	Cache Presence test	Cache
08	Setup low memory	64K
09	Early Cache Initialization	Cyrix CPU Cache
0A	Setup Interrupt Vector Table	
0B	Test CMOS RAM Checksum	CMOS
0C	Initialize Keyboard	
0D	Initialize Video Interface	
0E	Test Video Memory	
0F	Test DMA Controller 0	DMA 0 DMA
10	Test DMA Controller 1	DMA 1 DMA
11	Test DMA Page Registers	DMA DMA
12~13	Reserved	

16		
14	Test Timer Counter 2	8254
15	Test 8259-1 Mask Bits	8259 8259
16	Test 8259-2 Mask Bits	8259
17	Test Stuck 8259’s interrupt bits	8259
18	Test 8259 Interrupt Functionality	8259
19	Test stuck NMI Bits （Parity/IO	

	check	
1A	Display CPU Clock	CPU
1B-1E	Reserved	
1F	Set EISA Mode	EISA
20	Enable Slot 0	Slot 0
21-2F	Enable Slots 1-15	Slots 1 15
30	Size Base and Extended Memory	256K 640K 1M
31	Test Base and Extended Memory	ESC
32	Test EISA Extended Memory	slots EISA
33-3B	Reserved	
3C	Setup Enabled	BIOS
3D	Initialize &Install Mouse	
3E	Setup Cache Controller	Cache
3F	Reserved	
BF	Chipset Initialization	
40	Display virus protect disable or enabel	
41	Initialize Floppy Drive & Controller	
42	Initialize Hard Drive &Controller	
43	Detect & Initialize Serial/Parallel Ports	
44	Reserved	
45	Detect & Initialize Math Coprocessor	

	名 称	
46	Reserved	
47	Reserved	
48-4D	Reserved	
4E	Manufacturing POST loop or display message	
4F	Security Check	
50	Write CMOS	BIOS CMOS CMOS cache、NM c800:0 efff:0 ROM
51	Pre-boot Enable	
52	Initialze Option ROMs	
53	Initialize Time Value	BIOS 40H
60	Setup Virus Protect	
61	Set Boot Speed	
62	Setup Numlock	

63	Boot Attempt	INT 19H
BO	Spurious	
B1	Unclaimed NMI	NMI F1 NM
E1-EF	Setup Page	BIOS
FF	BOOT	

AMIBIOS 071596

AMIBIOS

D0	NMI is Disabled.CPU ID saved. Init code Checksum verification starting NMI，CPU
D1	To do DMA init ,Keyboard controller BAT test ,start memory refresh and going to 4GB flat mode DMA 4GB
D3	To start Memory sizing
D4	To comeback to real mode . Execute OEM patch. Set stack OEM
D5	E000 ROM enabled . Init code is copied to segment 0 and control to be transferred to segment 0. E000：0 ROM。：0 并：0
D6	Control is in segment 0. To check <CTRL><HOME> key and verify main BIOS Checksum. If either<CTRL><HOME>is pressed or main BIOS checksum is bad Go to check point E0 else goto check point D7 ：0 <CTRL><HOME>BIOS <CTRL><HOME> BIOS D7。
D7	To pass control to Interface Module.
D8	Main BIOS runtime code is to be decompressed. BIOS
D9	Control to be passed to main BIOS in shadow RAM BIOS
E0	OnBoard Floppy Controller(if any)is initialzed. To start base 512K memory test 512K
E1	To initialise interrupt vector table
E2	To initialise DMA and interrupt controllers DMA
E6	To enable floppy and timer IRQ,enable internal cache IRQ， cache
ED	Initialize floppy drive.

EE	Start looking for a diskette in drive A: and read 1st sector of the diskette
EF	Floppy read error
F0	Start searching ‘MIBOOT.ROM’ file in root directory MIBOOT.ROM
F1	AMIBOOT.ROM’ file not present in root directory. AMIBOOT.ROM
F2	Start reading FAT table and analyze FAT to find the clusters occupied by ‘AMIBOOT.ROM’ file AMIBOOT.ROM
F3	Start reading ‘MIBOOT.ROM’file cluster by cluster. MIBOOT.ROOM
F4	AMIBOOT.ROM’ file not of proper size AMIBOOT.ROM
F5	Disable internal cache cache
FB	Detect Flash type present. flash
FC	Erase Flash FLASH
FD	Program Flash FLASH
FF	Flash program successful.BIOS is going to restart FLASH， BIOS

在 F000 内存镜像区的实时代码

03	NMI is Disabled . To check soft reset /power- on NMI。
05	BIOS stack set . Going to disable Cache if any. BIOS 。cache
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done. CPU CPU
08	CMOS checksum calculation to be done next. CMOS
0B	Any initialization before keyboard BAT to be done next
0C	KB controller I/B free. To issue the BAT command to keyboard controller. BAT
0E	Any initialization after KB controller BAT to be done next.

	BAT

0F	Key board command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>,<END> key during power-on <INS><END>
12	To init CMOS if “Init CMOS in every boot ” is set or <END> key is pressed. Going to disable DMA and Interrupt controllers CMOS <END> DMA
13	Video display is disabled port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory Refresh line is toggling .Going to check 15us ON/OFF time
23	To read 8042 input and disable Megakey Green PC feature .Make BIOS segment Writeable
24	To do any setup before Int vector init .
25	Interrupt vector initialization about to begin. To clear password if necessary
27	Any initialization before setting video mode to be done .
28	Going for monochrome mode and color mode setting.
2A	Different BUSes init (system,static,output devices)to start if present.(please see appendix for details of defferent BUSes).
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	IF ega/vga not found then do display memory R/W test.
2F	Ega/vga not found .Display memory R/W test about to begin.

30	Display memory R/W test passed. About to look for the retrace checking.

31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over .Display mode to be set next.
37	Display mode set . Going to display the power on message.
38	Different BUSes init (input,IPL,general devices) to start if present.(please see Appendix for details of different BUSes)
39	Display different BUSes initialization error messages.(Please see appendix for details of different BUSes).
3A	New cursor position read and saved. To display the Hit <DEL> message.
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialze data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory
47	Pattern to be tested written in extended memory. Going to write patterns in base 640K memory
48	Pattern written in base memory .Going to findout amount of memory below 1M memory.
49	Amount of memory below 1M found and verified.Going to findout amount of memory above 1M memory

4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset.(if power on,go to check point#4Eh)
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared.(SOFT RESET)Going to save the memory size.(goto check point #52h).
4E	Memory size display started. (NOT SOFT RESET)About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing /initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity /NMI.
57	A20 address line ,parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit<DEL> message.
59	Hit<DEL> message cleared. <WAIT…> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA# 1 base register test
62	DMA# 1 base register test passed. To do DMA#2 base register test.

65	DMA#2 base register test passed. To program DMA unit 1 and 2
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started . clearing output buffer,checking for stuck key ,to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written , Global data init done . To check for lock-key.
84	Lock-key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete . To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared.About to do programming after setup
89	Programming after setup complete . Going to display power on screen message.
8B	First screen message displayed. <WAIT…> message displayed . PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start .
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.

91	Floppy setup complete . Hard disk setup to be done next.
95	Init of different BUSes optional ROMs from C800 to start.(please see Appendix-I for details fo different BUSes).
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Returm after setting timer and printer base address.Going to set the RS-232 base address
9B	Returned after RS-232 base address . Going to do any initialization before Coprocessor test 。
9C	Required initialized. Before Coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocesor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after coprocessor test is complete . Going to check extd keyboard, keyboard ID and num-lock
9F	Keyboard ID command to be issued.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set . To program memory wait states.
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control

	to optional ROM at E000.

A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned form E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	To build MP table if needed.
AC	To uncompress DMI data and execute DMI post init.
B0	System configuration is displayed
B1	Going to copy any code to specific area.
00	Copying of code to specific area done Going to give control to INT-19 boot loader